IN THE SPECIFICATION

1. Please insert the following replacement paragraph marked up to show changes made relative to the immediate prior version for the paragraph beginning at page 3, line 7, as follows:

--In order to program multiple bits on a single cell, multiple threshold levels must be programmed. Referring now to Figure 2A, a graphical representation of the correlation between the state of two bits and four threshold levels, according to the conventional art, is shown. As depicted in Figure 2A, the bit combination of '11' is represented by an un-programmed cell (e.g., $V_T=V_{T\ MIN}$=1V). The bit combination of '10' is represented by a first threshold voltage, V_{T1} (V_{T1}=1V). The bit combination of '01 is represented by a second threshold voltage, V_{T2} (V_{T2}=5V). The bit combination of '00' is represented by a third threshold voltage, V_{T3} (V_{T3}=7V). The plurality of threshold voltage levels are spread out between the minimum threshold voltage and the maximum threshold voltage that can be programmed and erased for a given memory device.--

2. Please insert the following replacement paragraph marked up to show changes made relative to the immediate prior version for the paragraph beginning at page 3, line 15, as follows:

--Referring now to Figure 2B, a graphical representation of the correlation between the state of three bits and eight threshold levels, according to the conventional art, is shown. As depicted in Figure 2B, the bit combination of '111' is represented by an un-programmed cell (e.g., $V_T=V_{T\ MIN}$=1V). The bit combinations of '110'-'000' are represented by the respective threshold voltages, V_{T1} - V_{T7} (e.g., V_{T1}=2V, V_{T2}=3V, V_{T3}=4V, V_{T4}=5V, V_{T5}=6V, V_{T6}=7V, and V_{T7}=8V).--

3. Please insert the following replacement paragraph marked up to show changes made relative to the immediate prior version for the paragraph beginning at page 4, line 1, as follows:

--Referring now to Figure 3, a graphical representation of the statistical deviation of multiple programmed threshold voltage levels according to the conventional art is shown. As depicted in Figure 3, a multiplicity of desired threshold voltages (e.g., V_T= 1V, 3V, 5V, 7V; and $V_T=V_{T\ MIN}$=1V) are shown. Each actual programmed threshold value will have a certain distribution 305, between a plurality of cells of a memory device. However, to ensure reliable operation of the memory device, the distribution 305 of a given threshold level must be separated from the next higher or lower threshold voltage level by a specified margin 310. The larger the deviation of a given threshold voltage level, the smaller the margin 310 is between adjacent threshold levels. Therefore, the distribution 305 in

programming a desired threshold value needs to be minimized. However, simply controlling the length of time that programming voltages are applied to the cell does not provide sufficient control of the distribution 305 of threshold values, to provide reliable operation of the memory device.--

4. Please insert the following replacement paragraph marked up to show changes made relative to the immediate prior version for the paragraph beginning at page 5, line 1, as follows:

--Referring now to Figure 5, a timing diagram of gate, drain, and threshold voltages in a MLC being programmed, according to the conventional art is shown. As depicted in Figure 5, a threshold voltage 505 (e.g., Vt2=5V) of a MLC is programmed. The threshold voltage 505 gradually rises from a minimum threshold voltage (e.g., $V_{T\ MIN}$=1V) to threshold voltage 505 (e.g., Vt2=5V). A series of voltage pulses 510 (e.g., Vg=8.5V) are applied to a gate, while another series of voltage pulses 515 (e.g., 5V) are applied to a drain of the MLC. Between each set of voltage pulses 520, 525, a verify process 530 is performed to determine the current threshold level.--

5. Please insert the following replacement paragraph marked up to show changes made relative to the immediate prior version for the paragraph beginning at page 9, line 1, as follows:

--In an exemplary implementation, a first gate voltage (e.g., V_G=4V) is applied along with a ramped drain voltage to program a first threshold voltage level (e.g., V_T=3V). A source voltage (e.g., V_S=0V) is also applied. The ramped drain voltage increases from a first level (e.g., 0V) toward a second level (e.g., 5V) over a period of time. When the drain current begins to decrease the first gate voltage and ramped drain voltage are removed (e.g., V_G=0V, V_D=0V). As a result, the threshold voltage is readily set to the desired level (e.g., V_T=3V).--

6. Please insert the following replacement paragraph marked up to show changes made relative to the immediate prior version for the paragraph beginning at page 10, line 13, as follows:

--Referring now to Figures 8A, 8B and 8C, timing diagrams of gate, drain and threshold voltages and drain current in a MLC being programmed, in accordance with one embodiment of the present invention, are shown. As depicted in Figure 8A, a first threshold voltage 805 (e.g., V_T=3V) is programmed by applying a first gate voltage 820 (e.g., V_G=4V) along with a ramped drain voltage 815. The ramped drain voltage 815 increases from a first level 816 (e.g., OV) toward a second level 817 (e.g., 5V) over a period of time. The drain current 810 rapidly increases as the drain voltage 815 increases. The

drain current 810 then begins to decrease 811 when the threshold voltage 805 reaches the desired level 806 (e.g., V_T=3V). The drain current 810 decreases as a result of the increasing threshold voltage 805 from $V_T=V_{T\ MIN}$ to V_T=3V effectively blocking the gate voltage 820 from inducing a conducting channel in the MLC. When the drain current 810 begins to decrease 811, the first gate voltage 820 and first drain voltage 815 are removed 818, 821 (e.g., V_G=0V, V_D=0V). As a result, the threshold voltage 805 is programmed to the level of voltage present on the gate (e.g., 4V) minus the minimum threshold voltage (e.g., $V_{T\ MIN}$=1V).

7. Please insert the following replacement paragraph marked up to show changes made relative to the immediate prior version for the paragraph beginning at page 11, line 1, as follows:

As depicted in Figure 8B, a second threshold voltage 830 (e.g., V_T=5V) is programmed by applying a second gate voltage 845 (e.g.. V_G=6V) at a level 846 along with a ramped drain voltage 840. The ramped drain voltage 840 increases from a first level 841 (e.g., V_D=0V) toward a second level 842 (e.g., V_D=5V) over a period of time, and drops at 843. The drain current 835 rapidly increases as the drain voltage increases 840. The drain current 835 then begins to decrease 836 when the threshold voltage 830 reaches the desired level (e.g., V_T=5V) 831. The drain current 835 decreases as a result of the

increasing threshold voltage 830 effectively blocking the gate voltage 845 from inducing a conducting channel in the MLC. When the drain current 835 begins to decrease 836, the second gate voltage 845 and first drain voltage 840 are removed 843, 846 (e.g., V_G=OV, V_D=OV). As a result, the threshold voltage 830 is programmed to the level of voltage present on the gate (e.g., 6V) minus the minimum threshold voltage (e.g., $\underline{V_T=V_{T_{MIN}}}$=1V) at level 831.

8. Please insert the following replacement paragraph marked up to show changes made relative to the immediate prior version for the paragraph beginning at page 11, line 12, as follows:

--As depicted in Figure 8C, a third threshold voltage 860 (e.g., V_T=7V) is programmed by applying a third gate voltage 875 (e.g.. V_G=8V) along with a ramped drain voltage 870. The ramped drain voltage 870 increases from a first level 871 (e.g., OV) toward a second level 872 (e.g., 5V) over a period of time. The drain current 865 rapidly increases as the drain voltage increases 870. The drain current 865 then begins to decrease 866 when the threshold voltage 860 reaches the desired level 861 (e.g., V_T=7V). The drain current 865 decreases as a result of the increasing threshold voltage 860 effectively blocking the gate voltage 875 from inducing a conducting channel in the MLC. When the drain current 865 begins to decrease 866, the third gate voltage and first drain voltage

are removed 873, 876 (e.g., V_G=OV, V_D=0V). As a result, the threshold voltage 860 is programmed to the level of voltage present on the gate (e.g., 8V) minus the minimum threshold voltage (e.g., $\underline{V_T=V_{T\ MIN}}$=1V).